

Design of High Efficiency Power Amplifiers using a Bare-die Approach

Paul Saad, Hossein Mashad Nemati, Mattias Thorsell, Kristoffer Andersson and Christian Fager
GigaHertz centre, Microwave Electronics Laboratory, Department of Microtechnology and Nanoscience (MC2)
Chalmers University of Technology, SE-412 96 Göteborg, Sweden
paul.saad@chalmers.se

ABSTRACT

This paper presents the design of two high efficiency power amplifiers, a class-J power amplifier (PA) using an LDMOS device and an inverse class-F PA using a GaN HEMT device.

The two PA designs are based on the same concept where bare-die devices are used instead of packaged devices in order to reduce parasitics and to facilitate harmonic impedance optimization at the transistor output reference plane.

The bare-die characterization procedure may be summarized as follows: First, the transistor chip is mounted in a high performance liquid crystal polymer package. The package is then placed in a high power test fixture during the characterization. The test fixture includes thru-reflect-line (TRL) calibration standards, which brings the reference plane to the tabs of the package. Finally, a model of the package is developed and used to de-embed the influence of the package from the measurements. This finally brings the reference plane of the measurements to the bond wires of the transistor die. These measurements have been used to develop bare die transistor models optimized for harmonically tuned and switched mode operation.

The fundamental and second-harmonic load impedances are optimized for maximum efficiency while other harmonics are blocked by a lowpass load network.

Designed at 1-GHz, the 10-W harmonically tuned Class-J power amplifier presents the state-of-the-art power-added efficiency (PAE) of 80%. The inverse class-F PA has been designed at 3.5 GHz, it shows an output power of 11-W and state-of-the-art PAE of 78%.

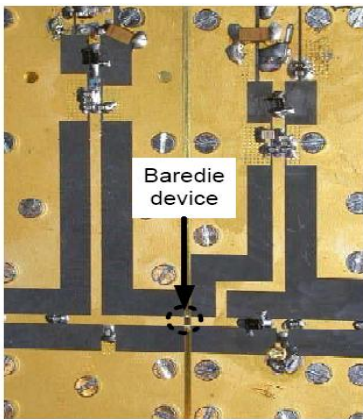


Fig. 1: Class-J power amplifier.

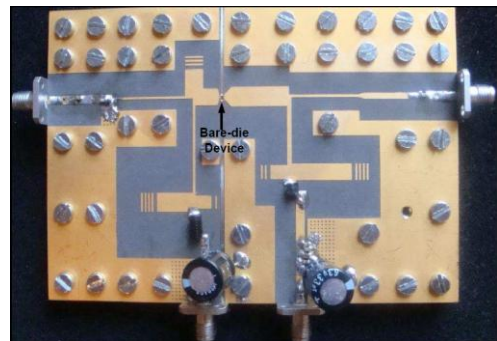


Fig. 2: Inverse class-F power amplifier.

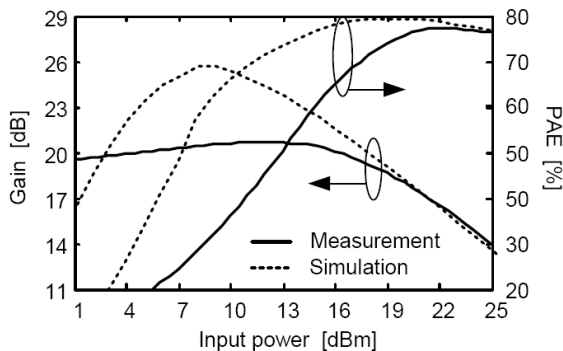


Fig. 3: Measured PAE and gain vs. input power level for the class-J PA.

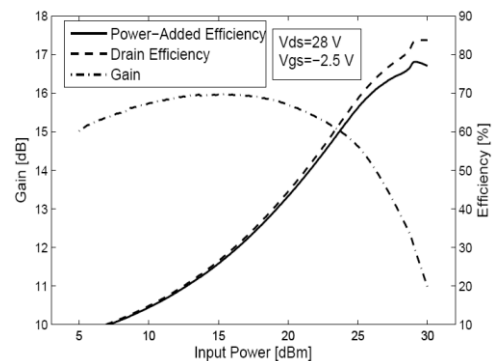


Fig. 4: Measured PAE, drain efficiency and gain vs. input power for the inverse class-F PA.

ACKNOWLEDGMENT

This research has been carried out in the GigaHertz Centre in a joint research project financed by Swedish Governmental Agency of Innovation Systems (VINNOVA), Chalmers University of Technology, Comheat Microwave AB, Ericsson AB, Infineon Technologies Austria AG, Mitsubishi Electric Corporation, NXP Semiconductors BV, Saab AB, and SP Technical Research Institute of Sweden.